VEER NARMAD SOUTH GUJARAT UNIVERSITY, SURAT
M.Sc. (I.T.) [Five Year Integrated Course]
B.Sc. (Information Technology)
Semester III

Effective from July 2004

Paper No : 303 **L: 4, T:0, P:0 Hrs**
Paper Title : Digital Electronics

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1. **Logic gates:-** Logic symbol, Timing Diagrams, Truth table Demorgan's first & second theorem. Interchangeability bubbled gates, Universal gates

2. **Boolean Laws & theorem,** duality theorem sum of product method & equation truth table, Karnaugh map for two three & four variables & it's simplification & NAND-NAND ckts, Don't care condition , product of sum method , & it's simplification . NOR - NOR ckts. & application of duality theorem.

3. **Data processing ckts.:-** Multiplexers, Nibble multiplexers, Demultiplexers decoders chip expansion, BCD to Decimal decoders, seven segment decoder, decoder driver IC's Encoders , decimal to BCD decoder, parity generator & checkers &its application (ROM, PROM, EPROM)

1. **Number system & Arithmetic ckts;-** Binary, Octal, hexadecimal ,Excess- 3 code, ASCII code, grey code conversion from one to another

2. **Binary addition & subtraction HALF adder, full adder , adder - subtracter ckts.**

3. **TTL & CMOS ckts.** Power Dissipation ,Propagation delay time ,TTL ckts ,two i/p TTL NAND gate , Inverter gate ,NOR gate ,Three state TTL devices , Schmitt Triggers, sinking and sousing , Loadings ,noise immunity, Positive and negative logic CMOS ckts , CMOS Inverter ,CMOS NAND , NOR gate.

7. **FLIP FLOPS -** Construction of flip flops using different gates , RS flip flops , D flip flop , Edge triggered D flip flop, clocked RS flip flop ,switching time , JK flip flop , JK master slave flip flop , Schmitt trigger.

8. **Shift Registers :** Types of Registers , Serial in Serial out , Serial in Parallel out , Parallel in Serial out , Parallel in Parallel out, Ring counter, Asynchronous counter 4, Binary up-down counter , Decoding gate , Synchronous counter , Mode 8 Parallel binary counter & up down counter , Parallel up down counter , Mod-3 counter , Mod-6 counters, Mod - 5 counters & C Decade counter, Shift counters, Digital clock.

9. **D/A & A/D conversion :** Variable Resistor Network , Binary Ladder , 4 bit D/A converter , dual slope A/D conversion.

Main Readings:

Digital Principles and Application : TATA Mc GRAW-HILL Edition by Albert Paul Malvino, Donald P. Leach